Electronic Version
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Claims

[c1] A self-aligned bipolar transistor structure comprising:
a raised extrinsic base including:
an outer region;
an inner extension region extending laterally inward from the outer region toward an emitter, the inner extension region horizontally non-overlapping the outer region; and
an intrinsic base positioned below the raised extrinsic base.

[c2] The transistor of claim 1, wherein the outer region is separated from an intrinsic base outer region by a dielectric layer.

[c3] The transistor of claim 1, wherein the inner extension region defines an opening into which the emitter is self-aligned to the raised extrinsic base.

[c4] The transistor of claim 1, further comprising a spacer between the inner extension region and the emitter.

[c5] The transistor of claim 1, wherein the emitter has a width less than 0.1 microns.

[c6] The transistor of claim 1, wherein the inner extension region has a non-uniform width.

[c7] The transistor of claim 1, wherein the outer region and the inner extension region each contact the intrinsic base.

[c8] The transistor of claim 7, wherein the outer region contacts the intrinsic base at a first location separated from a second location where the inner extension region contacts the intrinsic base.

[c9] The transistor of claim 7, wherein the outer region also contacts an intrinsic base outer region that is positioned over a shallow trench isolation.

[c10] The transistor of claim 1, wherein only the inner extension region contacts the intrinsic base.

[c11] The transistor of claim 1, wherein the outer region has a first doping concentration and the inner extension region has a second doping concentration, and the second doping concentration is different than the first doping concentration.

[c12] A transistor comprising:
a raised extrinsic base including:
an outer region that contacts an intrinsic base at a first

location; and

an inner extension region distinct from the outer region, the inner extension region contacting the intrinsic base at a second location laterally inward and separated from the first location.

[c13] The transistor of claim 12, wherein the outer region has a first doping concentration and the inner extension region has a second doping concentration, and the second doping concentration is higher than the first doping concentration.

[c14] The transistor of claim 12, wherein the outer region includes a polysilicon and the inner extension region includes one of silicon and polysilicon.

[c15] A method of fabricating a self-aligned bipolar transistor, the method comprising the steps of:

forming a first opening to expose a first extrinsic base region;

generating a dummy pedestal within the first opening, the dummy pedestal having a surrounding trench;

forming an extrinsic base extension region in the trench, the extrinsic base extension region connecting the first extrinsic base region to an intrinsic base;

removing the dummy pedestal to form an emitter opening; and

forming an emitter in the emitter opening.

[c16] The method of claim 15, wherein the generating step includes:
depositing a sacrificial layer in the first opening to form a second opening that is smaller than the first opening, the second opening defining a size of the dummy pedestal;
depositing a filler material in the second opening; and
removing the sacrificial layer and the filler material to generate the dummy pedestal and the trench.

[c17] The method of claim 15, wherein the step of forming the extrinsic base extension region includes providing one of silicon and polysilicon, and wherein the first extrinsic base region includes one of silicon and polysilicon having a different doping concentration than the extrinsic base extension region.

[c18] The method of claim 17, wherein the extrinsic base extension region has a higher doping concentration than the first polysilicon.

[c19] The method of claim 15, wherein the emitter forming step includes:
forming a spacer on a sidewall of the emitter opening; and

depositing a third polysilicon in the emitter opening to form the emitter.

[c20] The method of claim 15, further comprising the following steps prior to the first opening forming step:
depositing a first dielectric layer;
depositing the first polysilicon over the first dielectric layer; and
depositing a second dielectric layer over the first polysilicon,
wherein the first opening is formed to the first dielectric layer.

[c21] The method of claim 20, wherein the emitter forming step further includes removing the first dielectric layer within the first opening.

[c22] The method of claim 20, further comprising the step of forming a cap for the extrinsic base extension region in the second dielectric layer.

[c23] The method of claim 20, further comprising the step of thermally growing a thermal oxide layer prior to depositing the first dielectric layer; and wherein the generating step includes:
depositing a sacrificial layer in the first opening to form a second opening that is smaller than the first opening,

the second opening defining a size of the dummy pedestal;

depositing a filler material in the second opening;

removing the sacrificial layer and the filler material to generate the dummy pedestal and the surrounding trench, wherein the surrounding trench is formed to the thermal oxide layer;

etching the first dielectric layer to form a ledge under the first extrinsic base region; and

etching the thermal oxide layer to enlarge the ledge and extend the surrounding trench to the intrinsic base.

[c24] The method of claim 15, wherein the generating step includes:

depositing a sacrificial layer in the first opening;

masking an area to become the dummy pedestal in the first opening; and

removing the sacrificial layer outside of the area and within the first opening to form the dummy pedestal and the surrounding trench.

[c25] The method of claim 24, wherein the mask and the first opening are misaligned.

[c26] A method of fabricating a self-aligned bipolar transistor, the method comprising the steps of:

forming a first opening, using lithography, to expose an

outer extrinsic base region;
depositing a sacrificial layer in the first opening;
forming, using lithography, a dummy pedestal in the sacrificial layer with a surrounding trench in the first opening;
forming one of silicon and polysilicon in the trench to form an inner extrinsic base extension region connecting the outer extrinsic base region to an intrinsic base;
removing the dummy pedestal to form an emitter opening; and
forming an emitter in the emitter opening.

[c27] The method of claim 26, wherein the lithography used to form the dummy pedestal and the trench is misaligned with the first opening.

[c28] A method of fabricating a self-aligned bipolar transistor, the method comprising the steps of:
forming an opening in an outer extrinsic base region;
generating an inner extrinsic base extension region connecting the outer extrinsic base region to an intrinsic base, the outer extrinsic base region and the inner extrinsic base region forming a raised extrinsic base; and
forming a self-aligned emitter within the inner extrinsic base extension region and to the raised extrinsic base.

[c29] The method of claim 28, wherein the outer extrinsic base

region has a different doping concentration than the inner extrinsic base extension region.

[c30] The method of claim 28, wherein the self-aligned emitter has a sub-lithographic dimension.